REMARKS

STATUS OF THE CLAIMS

Claims 14-34 are pending in the application.

Claims 14-20, 33 and 34 remain rejected under 35 U.S.C. 102(b) as being anticipated by Alpert et al., U.S. Patent No. 5,740,413.

Claims 21-32 remain rejected under 35 U.S.C. 102(e) as being anticipated by Alverson et al., U.S. Patent No. 6,480,818.

According to the foregoing, the claims are amended, and thus remain pending for reconsideration, which is respectfully requested.

No new matter has been added.

The independent claims 14, 15, 33 and 34 are amended taking into consideration the Examiner Response to Arguments comments, namely by providing "a condition determination section for determining whether an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition of said conditional instruction (claim 1). It s believed the amendments place the application in condition for allowance by overcoming Alpert and Alverson, which is respectfully requested.

The amended independent claims clarify that a break-interrupt is generated when as an instruction of a designated address "an instruction located at an address specified as a break point address" is executed as a condition of a conditional instruction, such that the condition of the conditional instruction is satisfied by execution of the instruction of the designated address.

Alpert discusses that a branch breakpoint is generated in response to the execution of an instruction causing a branch to be taken. Since Alpert doesn't consider performing an AND operation to a branch breakpoint unit and an address breakpoint unit, when the branch-trace mode is enabled, in Alpert the processor generates ***a break each time an instruction that causes a branch to be taken is executed***. The Response to Arguments also refers to US Patent no. 5,659,679 (Alpert-2) cross referenced by Alpert describing the branch breakpoint unit 190, however, Alpert-2 also suffers from the same deficiency as Alpert-1, namely Alpert-2 discusses profiling when executing an instruction which instructs the processor to transfer flow of execution to another instruction (Abstract), so Alpert-2 also generates a break ***each time an instruction that causes a branch to be taken is executed***, which also fails to disclose

expressly or inherently the claimed "a condition determination section for determining whether an instruction of a designated address is executed as satisfying a branch condition of said conditional instruction; and a control section for controlling a break-interrupt based upon a breakpoint detection result from said break detection section and execution of the instruction of the designated address according to a branch condition determination result from said condition determination section."

Further, it is readily apparent Alverson's conditional breakpoint that merely refers to whether the nub has designated the breakpoint as valid or invalid, fails to disclose expressly or inherently the amended claims, namely "determining whether an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition of said conditional instruction; and … controlling a break-interrupt based upon a breakpoint detection result from said break detection section and execution of the instruction of the designated address according to a branch condition determination result from said condition determination section."

A prima facie case of anticipation based upon Alpert or Alverson cannot be established, because Alpert and Alverson fail to disclose, either expressly or inherently, that a break-interrupt is generated when an instruction for execution is an instruction of ***a designated conditional instruction*** (instruction address) ***and*** the condition of the conditional instruction is satisfied. In other words, for a break-interrupt, the language of the claims requires both (1) and (2), namely "determining whether ***an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition*** of said conditional instruction; and … controlling a break-interrupt based upon (1) a breakpoint detection result from said break detection section and (2) execution of the instruction of the designated address according to a branch condition determination result from said condition determination section."

In view of the amendments and remarks, withdrawal of the rejections and allowance of claims is respectfully requested.

CONCLUSION

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,
STAAS & HALSEY LLP

/Mehdi D. Sheikerz/

Date: October 24, 2008

By: _____
Mehdi D. Sheikerz
Registration No. 41,307

1201 New York Ave, N.W., 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501